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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,069	04/13/2004	John Stephen Drewery	101.113	7008

43023 7590 11/02/2007

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EXAMINER	
VINH, LAN	

ART UNIT	PAPER NUMBER
1792	

MAIL DATE	DELIVERY MODE
11/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/824,069	DREWERY ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1792	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-26, 28-45* is/are rejected.

7)☒ Claim(s) *6 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *082205*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 7-9, 11-16, 39 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsuda et al (US 2004/0226827)

Matsuda discloses a method of manufacturing electronic device. The method comprises the steps of:

applying an insulating layer 1 (polyimide) to a base layer 2 of a workpiece (page 2, paragraph 0037-0038), which reads on applying a resist layer to a base layer of a workpiece since page 12 of the instant application discloses "the terms "resist", "resist layer" are used broadly to mean a layer that can be formed and patterned"

patterning said layer 1/resist layer to form a concave portion/recessed region and an adjacent planar portion/field region in the layer 1 (page 3, paragraph 0050; fig.1A)

then depositing a metal seed layer 5 on the workpiece, including in said concave/recessed region and on said planar/field region (page 3, paragraph 0050)

then causing a plating accelerator 6 to become attached to said metal seed layer 5 selectively in said concave/recessed region, with relatively little or no accelerator

attached to said metal seed layer in said planar/field region, thereby forming an acceleration region in said concave/recessed region (page 3, paragraph 0050; fig. 1B)

then plating copper 8 on said workpiece, wherein said accelerator selectively attached in said acceleration region increases a rate of copper plating in said acceleration region relative to a rate of copper plating in said field region (page 4, paragraph 0082)

Regarding claim 2, Matsuda discloses continuing plating copper until an accelerated thickness of plated copper in said concave/acceleration region is at least 3 pm thicker than a field thickness of copper in said field region (page 9, paragraph 0116)

Regarding claim 3, Matsuda discloses a step of removing copper from said field region after said processes of plating copper (page 3, paragraph 0052)

Regarding claim 4, Matsuda discloses removing copper from said field region form a wiring line 8 having a wire width at least two times greater than a wire thickness (fig. 2)

Regarding claims 7, 11, Matsuda discloses the steps of applying an accelerator film on said metal seed layer; and then selectively removing at least a portion of said accelerator film from said metal seed layer in said field region (page 3, paragraphs 0050, 0052)

Regarding claims 8-9, Matsuda discloses applying an accelerator film is conducted using an accelerator solution; and the plating copper is conducted using a plating solution, wherein said accelerator solution comprises a greater concentration of said accelerator than said plating solution (page 3, paragraph 0048)

Regarding claims 12-14, Matsuda discloses removing at least a portion of said accelerator by contacting said workpiece surface with a web/pad that selectively

removes said accelerator film from said field region prior to plating copper (page 3, paragraph 0053)

Regarding claims 15-16, Matsuda discloses applying the accelerator to the workpiece during the plating process (page 4, paragraph 0062)

Regarding claim 39, Matsuda discloses continuing depositing metal until the thickness of plated copper in the concave/acceleration region is thicker than the copper in the planar/field region (fig. 6)

2. Claims 17-20, 22-23, 25-26, 28, 40-42, 44-45 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsuda et al (US 2004/0226827)

Matsuda discloses a method of manufacturing electronic device. The method comprises the steps of:

applying an insulating layer 1 (polyimide) to a base layer 2 of a workpiece (page 2, paragraph 0037-0038), which reads on applying a resist layer to a base layer of a workpiece;

patterning said layer 1/resist layer to form a concave portion/recessed region and an adjacent planar portion/field region in the layer 1 (page 3, paragraph 0050; fig.1A)

then depositing a metal seed layer 5 on the workpiece, including in said concave/recessed region and on said planar/field region (page 3, paragraph 0050)

then causing a plating accelerator 6 to become attached to said metal seed layer 5 selectively in said concave/recessed region, with relatively little or no accelerator attached to said metal seed layer in said planar/field region, thereby forming an

acceleration region in said concave/recessed region (page 3, paragraph 0050; fig. 1B) then plating copper 8 on said workpiece, wherein said accelerator selectively attached in said acceleration region increases a rate of copper plating in said acceleration region relative to a rate of copper plating in said field region (page 4, paragraph 0082)

Regarding claim 18, Matsuda discloses continuing plating copper until an accelerated thickness of plated copper in said concave/acceleration region is at least 3 pm thicker than a field thickness of copper in said field region (page 9, paragraph 0116)

Regarding claim 19, Matsuda discloses a step of removing copper from said field region after said processes of plating copper (page 3, paragraph 0052)

Regarding claim 20, Matsuda discloses removing copper from said field region form a wiring line 8/metal structure having a wire width at least two times greater than a wire/metal structure thickness (fig. 2)

Regarding claim 22, Matsuda discloses the steps of applying an accelerator film on said metal seed layer; and then selectively removing at least a portion of said accelerator film from said metal seed layer in said field region (page 3, paragraphs 0050, 0052)

Regarding claim 23, Matsuda discloses applying an accelerator film is conducted using an accelerator solution; and the plating copper is conducted using a plating solution, wherein said accelerator solution comprises a greater concentration of said accelerator than said plating solution (page 3, paragraph 0048)

The limitations of claims 25-26, 28 have been discussed above

Regarding claims 40-41, Matsuda discloses continuing depositing metal until the thickness of plated copper in the concave/acceleration region is thicker than the copper in the planar/field region (fig. 6)

Regarding claim 42, Matsuda discloses depositing metal containing barrier layer 29 in the concave/recessed region before depositing the seed layer 30 (page 8, paragraph 0107)

Regarding claims 44-45, Matsuda discloses forming the seed layer by electrolytic deposition (page 3, paragraph 0050)

3. Claims 29-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsuda et al (US 2004/0226827)

Matsuda discloses a method of manufacturing electronic device. The method comprises the steps of:

applying a liquid accelerator solution having accelerator molecules on the entire workpiece to form an accelerator film on said workpiece (page 3, paragraph 0045; page 4, paragraph 0062), which reads on globally applying an accelerator to a workpiece to form a global accelerator film on said workpiece;

selectively removing a portion of said accelerator film from said workpiece to form a concave/acceleration region and a planar/non-activated region on said workpiece, said acceleration region comprising accelerator at a higher concentration than in said non-activated region (page 3, paragraph 0050; fig. 1B)

then using a plating technique to deposit metal on said workpiece, wherein said

accelerator at higher concentration in said acceleration region increases a rate of metal plating in said acceleration region relative to a rate of metal plating in said non-activated region (page 4, paragraph 0062)

Regarding claim 31, Matsuda discloses after said applying said liquid accelerator solution, removing liquid accelerator solution from said workpiece without substantially removing said accelerator film from said workpiece (page 3, paragraph 0053)

Regarding claim 32, Matsuda discloses removing liquid accelerator solution from said workpiece comprise rinsing said workpiece with pure water/liquid solvent, said liquid solvent having a lower concentration of accelerator than a concentration of accelerator in said liquid accelerator solution (page 3, paragraph 0053)

Regarding claim 33, Matsuda disclose irradiating the workpiece with UV during removing the accelerator (page 4, paragraph 0057), which reads on drying said workpiece

Regarding claims 34-35, plating copper 8 on said workpiece, wherein said accelerator selectively attached in said acceleration region increases a rate of copper plating in said acceleration region relative to a rate of copper plating in said field region (page 4, paragraph 0082)

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Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 21, 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over (US 2004/0226827) in view of Nakamura et al (US 2001/0013472)

Matsuda method has been described above. Unlike the instant claimed inventions as per claims 5, 21, 43, Matsuda fails to disclose a step of conducting a wet etch to remove copper from the field region

Nakamura discloses a method of plating for filling via hole comprises a step of conducting a wet etch to remove copper from the substrate (page 3, paragraph 0051)

One skilled in the art at the time the invention was made would have found it obvious to modify Matsuda method by conducting a wet etch to remove copper from the substrate as per Nakamura since Nakamura discloses that the removal of copper plating can be achieved by immersing the substrate in a solution for etching copper (page 3, paragraph 0051)

5. Claims 10, 24, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over (US 2004/0226827) in view of Nakamura et al (US 2001/0013472)

Matsuda method has been described above. Unlike the instant claimed inventions as per claims 10, 24, 38, Matsuda fails to specifically disclose that the accelerator solution comprises accelerator molecules selected from the group consisting of 2-mercaptoethane sulfonic acid (MESA), 3-mercapto-l-propane sulfonic acid (MPSA), 3-mercaptopropionic acid, mercaptopyruvate, 3-mercapto-2-butanol, 1- thioglycerol,

dimercaptopropane sulfonic acid (DMPSA), dimercaptoethane sulfonic acid (DMESA), and salts thereof

Nakamura discloses a method of plating for filling via hole by using a plating solution contains a plating promoter/accelerator comprises of sodium 3-mercapto-l-propane sulfonic acid (page 4, paragraph 0062)

One skilled in the art at the time the invention was made would have found it obvious to modify Matsuda method by using a plating solution contains a plating promoter/accelerator comprises of sodium 3-mercapto-l-propane sulfonic acid as per Nakamura because Nakamura discloses that the solution containing the plating promoter makes it easy to deposit copper on a substrate at a lower voltage than that required in the case of a plating solution containing no plating promoter (page 4, paragraph 0062)

Allowable Subject Matter

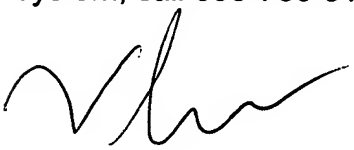
6. Claims 6, 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



LV
October 24, 2007